ATM cell buffer circuit and priority order allocating method at ATM switching system

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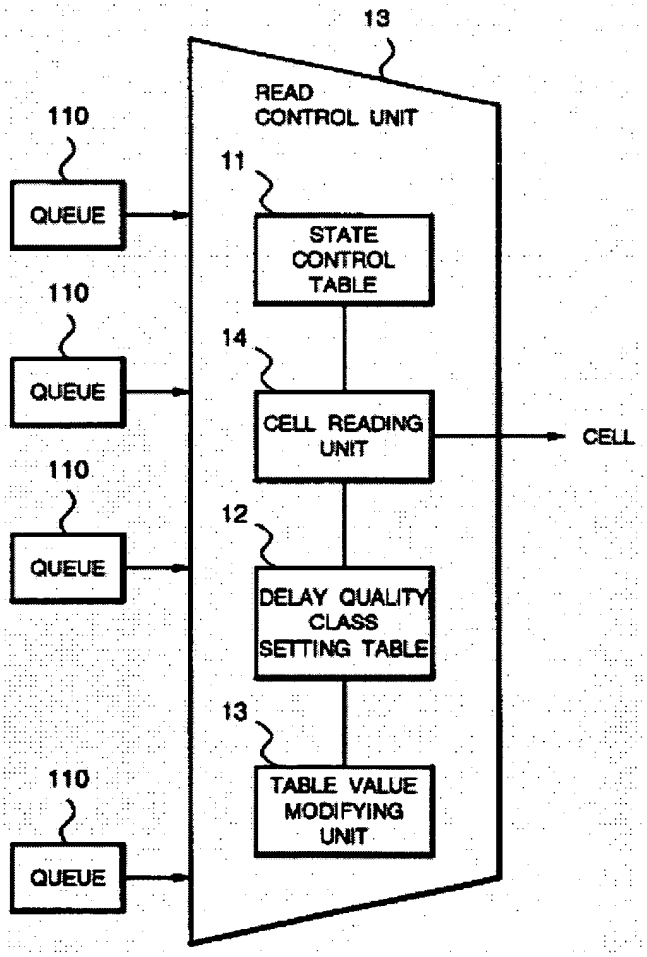
An ATM cell buffer circuit including an output buffer type ATM switch for switching ATM cells and an input buffer unit provided for each line, read control means of the input buffer unit for reading a cell from a queue which temporarily stores an input cell and transmitting the same to the output buffer type ATM switch including a state control table, a delay quality class setting table for setting cell reading priority for each priority class assigned to an input cell, table value modifying means for modifying a set value of the delay quality class setting table as required and cell reading means for determining priority order to read a cell based on the delay quality class setting table and the state control table.



ATM cell buffer circuit and priority order allocating method at ATM switching system

Description of correspondent: **US6301253**

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an ATM cell switching device and, more particularly, to an ATM cell buffer circuit and a priority order allocating method at an ATM switching system which conduct priority control of the order of ATM cell transmission at the time of occurrence of ATM cell congestion.

2. Description of the Related Art

One of conventional ATM cell buffer circuits of this kind is, for example, the ATM cell buffer circuit disclosed in Japanese Patent Laying-Open (Kokai) No. Heisei 7-297840, entitled "Priority Controlling Method at Output Buffer Type ATM Switch". The ATM cell buffer circuit recited in the literature, which is disposed at an input line unit located at the preceding stage of a switch unit in an ATM switching system, conducts reduction of a cell discard rate and control of a cell transmission delay in the ATM switching system according to a cell discard rate and a cell transmission delay time limit required for each connection.

FIG. 4 is a block diagram showing structure of a conventional ATM cell buffer circuit. As illustrated in FIG. 4, the ATM buffer circuit includes an input buffer unit 100 provided for each line and an output buffer type ATM switch 200. The input buffer unit 100 conducts priority control based on a discard quality class and a delay quality class assigned to an input cell as a parameter. The output buffer type ATM switch 200 conducts switching based on routing information (output port number and other information) stored in an input cell. The switch also outputs a cell according to a transmission capacity of the output side.

The output buffer type ATM switch 200 includes a switch unit 210, output buffer units 220 and congestion monitoring units 230 connected to the respective output buffer units. The switch unit 210 switches (self-switching) a cell received from each input buffer 100 through an input port to a predetermined output port based on routing information assigned to the cell. The output buffer unit 220 is provided for each output port of the switch unit 210 and has a plurality of buffer memories therein corresponding to the order of priority based on delay quality classes. The congestion monitoring unit 230 is provided for each output buffer 220 and outputs an output buffer threshold value exceeding signal S0 when the amount of cells accumulated in the buffer memory in each output buffer unit 220 exceeds a predetermined threshold value. The output buffer threshold value exceeding signal S0 output from the congestion monitoring unit 230 is fed back to the input buffer unit 100.

The input buffer unit 100 includes a write control unit 120, queues 110 and a read control unit 130. The queue 110 is a logic queue virtually provided, in a buffer memory, corresponding to a delay quality class and each output port of the switch unit 210 for temporarily storing an input cell. The write control unit 120 writes an input cell to a queue 110 corresponding to a delay quality class and an output port number assigned to the input cell according to the amount of cells accumulated in each queue 110. The read control unit 130 receives input of the amount of cells accumulated in each queue 110 and an output buffer threshold value exceeding signal S0 output from the congestion monitoring unit 230, and reads and transmits a cell from a predetermined queue 110 to the switch unit 210 in response to the output buffer threshold value exceeding signal S0.

FIG. 5 is a diagram for use in explaining reading priority order based on delay quality classes in the ATM cell buffer circuit of FIG. 4. With reference to FIG. 5, a discard quality class and a delay quality class assigned to an input cell are represented by a matrix of priority class CL (x, y). The figure shows that the lower the discard quality class x assigned to an input cell is, the more liable the cell is to be discarded to have a higher discard rate and that to the contrary, the higher the discard quality class x is, the less liable the cell is to be discarded to have a lower discard rate. The figure also shows that the lower a delay quality class y is, the harder the cell is to be read to have a longer delay time and that to the contrary, the higher

the delay quality class y is, the easier the cell is to be read to have a shorter delay time.

Description will be next made of operation of the read control unit 130 in the input buffer unit 100 with reference to FIG. 5. At each input buffer unit 100, the queues 110 are logically divided into (the number of output ports of the switch unit 210: N).times.(the number of initial delay quality classes: y-2). Assuming that delay quality classes in FIG. 5 are `1` to `4`, an initial delay quality class of each queue 110 is fixedly determined to be `2` or `3` at the initial setting of the ATM switch. This value can not be modified.

The read control unit 130 has a state control table to be referred to for the reading of cells from the queues 110 and controls such that when the number of cells accumulated in each queue 110 exceeds a threshold value, a delay quality class of the queue 110 is upgraded from `2` to `3` or from `3` to `4` and on the reception of an output buffer threshold value exceeding signal from the congestion monitoring unit 230, the value of a delay quality class of a queue 110 corresponding to the output port in question is reduced to "1". Cell reading is conducted by sequentially confirming whether cells are accumulated in the queues 110 in the descending order of the classes, starting with a queue 110 whose delay quality class is `4`, the highest, and reading cells of a queue 110 of a class in question when cells are accumulated. When there exist a plurality of queues 110 of the same delay quality class where cells are accumulated, one queue 110 is equally selected under round robin priority control, from which cells are read. When no cell is accumulated in queues 110 whose delay quality class values are `4`, `3`, and `2` and cells are accumulated in a queue 110 whose delay quality class value is `1`, idle cells are transmitted to the switch unit 210 without execution of cell reading from the queue 110.

The above-described conventional ATM cell buffer circuit, however, has a drawback that in a state where services are being provided without using all the delay quality classes which the ATM cell switching device has, when service of a new delay quality class is to be added, if the delay quality class to be assigned to the additional service fails to coincide with an unused delay quality class, such laborious work is necessary as suspension of the service of a delay quality class which is already being provided or re-routing of connections because relative positioning of the priority for reading cells from the respective queues 110 is fixed.

Further description will be made with respect to a concrete example. It is assumed that the respective queues 110 at the input buffer unit 100 have three delay quality classes which are referred to as Qos#1, Qos#2 and Qos#3, respectively. Assuming that the number of delay quality classes of the queues 110 is three, a value of the delay quality class y managed by the read control unit 130 ranges from `1` to `5` and a value of the initial delay quality class to be assigned to the three delay quality classes will accordingly range from `2` to `4`. If at the start of the services, only two of the three delay quality classes need to be used and when at the time of addition of an unused delay quality class, its priority over the existing two delay quality classes is unknown, conditions of using two classes among the initial delay quality class values from `2` to `4` can not be determined. Therefore, it is assumed that a delay quality class with the value of `2` whose reading priority is low is not to be used and delay quality classes with the values of `3` and `4` are to be used. As described above, it is also assumed in the conventional art that correspondence between delay quality classes Qos#1, Qos#2 and Qos#3 and initial delay quality class values from `2` to `4` at each queue 110 is fixed and that the initial delay quality class value of Qos#1 is `2`, the initial delay quality class value of Qos#2 is `3` and the initial delay quality class value of Qos#3 is `4`. In other words, at the start of the service, queues 110 having the delay quality classes Qos#2 and Qos#3 are to be used and a queue 110 having the delay quality class Qos#1 is yet to be used.

Under these conditions, when with respect to, for example, a queue 110 of the delay quality class Qos#2 whose service is being already provided, a total of 300 connections are routed, 100 for a queue 110 directed to a switch output port [0], 100 for a queue 110 directed to a switch output port [1] and 100 for a queue 110 directed to a switch output port [2], the following procedure is necessary to set a delay quality class of the service to be newly started between two delay quality classes whose services are being already provided.

First, temporarily stop services (cell conduction) at all of the 300 connections for the queue 110 of the delay quality class Qos#2. Then, newly set the routing of the 300 connections to a queue 110 of the delay quality class Qos#1 directed to the switch output port [0], a queue 110 of the same class directed to the switch output port [1] and a queue 110 of the same class directed to the switch output port [2]. Then, resume the services (cell conduction), and further, set routing of connections for the new service to queues 110 of the delay quality class Qos#2 directed to the respective switch output ports to start the new service.

SUMMARY OF THE INVENTION

An object of the present invention is to provide an ATM cell buffer circuit and a priority order allocating method at an ATM switching system enabling addition of service of a new delay quality class without stopping the existing services, irrespective of the positioning of the new delay quality class of the service.

According to the first aspect of the invention, an ATM cell buffer circuit which conducts priority control of the order of transmission of ATM cells at the time of occurrence of ATM cell congestion, comprises
an output buffer type ATM switch for switching ATM cells and an input buffer unit provided for each line,
the output buffer type ATM switch comprises
switching means for switching a cell received from each input buffer unit through an input port to a predetermined output port based on routing information assigned to the cell,
output buffer means provided for each output port of the switching means and having a plurality of buffer memories therein corresponding to the order of priority based on delay quality classes, and
congestion monitoring means provided for each the output buffer means for, when the amount of cells accumulated at the buffer memory in the output buffer means exceeds a threshold value, notifying the input buffer unit of the excess, and
the input buffer unit comprises
queues provided divisionally in terms of logic corresponding to the respective output ports of the switching means of the output buffer type ATM switch and the respective cell reading priority classes and disposed at the input ports of the output buffer type ATM switch for temporarily storing an input cell,
write control means for queuing the input cell to its corresponding queue based on routing information assigned to the input cell, and
read control means for selecting a queue whose cell reading priority order is the highest among the queues where cells are accumulated based on the amount of cells accumulated at each the queue and the notification from the congestion monitoring means, reading a cell from the selected queue and transmitting the same to the switching means at each timing of transmitting a cell to the output buffer type ATM switch,
wherein the read control means comprises
a state control table to be referred to for the reading of a cell from the queue,
a delay quality class setting table for setting cell reading priority for each priority class indicative of a discard quality class and a delay quality class assigned to an input cell,
table value modifying means for modifying a set value of the delay quality class setting table as required, and
cell reading means for determining the order of priority to read a cell based on the delay quality class setting table and the state control table.

In the preferred construction, the delay quality class setting table stores the order of reading priority of each delay quality class at the queues logically divided into (the number of output ports of the switching means: N).times.(the number of delay quality classes: y-2), a set value of which can be arbitrarily modified in the range from `2` to `y-1`.

In the preferred construction, the table value modifying unit time-divisionally provides, within a time for transmitting one cell from the input buffer unit to the switching means of the output buffer type ATM switch, a time slot for modifying a set value of the delay quality class setting table and a time slot for selecting the queue which will transmit a cell to the switching means to modify a set value of the delay quality class setting table.

In another preferred construction, the delay quality class setting table stores the order of reading priority of each delay quality class at the queues logically divided into (the number of output ports of the switching means: N).times.(the number of delay quality classes: y-2), a set value of which can be arbitrarily modified in the range from `2` to `y-1`, and the table value modifying unit time-divisionally provides, within a time for transmitting one cell from the input buffer unit to the switching means of the output buffer type ATM switch, a time slot for modifying a set value of the delay quality class setting table and a time slot for selecting the queue which will transmit a cell to the switching means to modify a set value of the delay quality class setting table.

In another preferred construction, the read control means, at the time of reading of a cell from the queue, when there exists only one the queue of the same priority class where cells are accumulated, reads a cell from the queue and transmits the same to the switching means, when there exit a plurality of the queues

of the same priority class where cells are accumulated, equally selects one the queue by round robin priority control to read a cell and transmit the same to the switching means, and when no cell is accumulated in each queue, transmits an idle cell to the switching means.

According to the second aspect of the invention, a priority order allocating method of conducting priority control of the order of transmission of ATM cells at the time of occurrence of ATM cell congestion in an ATM switching system, comprising the steps of:
queuing an input cell to its corresponding queue based on routing information assigned to the input cell,
selecting a queue whose cell reading priority order is the highest among the queues where cells are accumulated based on the amount of cells accumulated at each the queue and reading a cell from the selected queue at each timing of transmitting a cell,
switching the cell read from the selected queue to a output port based on routing information assigned to the cell, and
detecting cell congestion of the cell switched to the output port and notifying the reading step of the cell congestion as a congestion information,
wherein the reading step includes
setting cell reading priority for each priority class indicative of a discard quality class and a delay quality class assigned to an input cell to make a delay quality class setting table,
modifying a set value of the delay quality class setting table as required,
determining the order of priority to read a cell based on the delay quality class setting table and the congestion information.

In this case, at the table value modifying step, a time slot for modifying a set value of the delay quality class setting table and a time slot for selecting the queue which will transmit a cell are time-divisionally provided at each timing of transmitting a cell.

According to another aspect of the invention, a computer readable memory having a control program for conducting priority control of the order of transmission of ATM cells at the time of occurrence of ATM cell congestion in a ATM system, the control program comprising the steps of:
queuing an input cell to its corresponding queue based on routing information assigned to the input cell;
selecting a queue whose cell reading priority order is the highest among the queues where cells are accumulated based on the amount of cells accumulated at each the queue and reading a cell from the selected queue at each timing of transmitting a cell;
switching the cell read from the selected queue to a output port based on routing information assigned to the cell; and
detecting cell congestion of the cell switched to the output port and notifying the reading step of the cell congestion as a congestion information;
wherein the reading step includes
setting cell reading priority for each priority class indicative of a discard quality class and a delay quality class assigned to an input cell to make a delay quality class setting table,
modifying a set value of the delay quality class setting table as required,
determining the order of priority to read a cell based on the delay quality class setting table and the congestion information.
Other objects, features and advantages of the present invention will become clear from the detailed description given herebelow.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be understood more fully from the detailed description given herebelow and from the accompanying drawings of the preferred embodiment of the invention, which, however, should not be taken to be limitative to the invention, but are for explanation and understanding only.

In the drawings:

FIG. 1 is a block diagram showing structure of a read control unit of an ATM cell buffer circuit according to one embodiment of the present invention.

FIG. 2 is a diagram showing structure of a delay quality class setting table according to the present embodiment.

FIG. 3 is a timing chart showing a relationship between internal operation of the read control unit and cell

transmission processing in the present embodiment.

FIG. 4 is a block diagram showing structure of the ATM cell buffer circuit.

FIG. 5 is a diagram showing reading priority order based on delay quality classes.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The preferred embodiment of the present invention will be discussed hereinafter in detail with reference to the accompanying drawings. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be obvious, however, to those skilled in the art that the present invention may be practiced without these specific details. In other instance, well-known structures are not shown in detail in order to unnecessary obscure the present invention.

An ATM cell buffer circuit according to one embodiment of the present invention, similarly to the conventional ATM cell buffer circuit shown in FIG. 4, includes an input buffer unit 100 provided for each line and an output buffer type ATM switch 200. The output buffer type ATM switch 200 includes a switch unit 210, an output buffer unit 220 and a congestion monitoring unit 230 connected to each output buffer unit, and the input buffer unit 100 includes a write control unit 120, a queue 110 and a read control unit 10. Since these components, except for the read control unit 10, are the same as their counterpart components in the conventional ATM cell buffer circuit shown in FIG. 4, the same reference numerals are allotted thereto to omit their description.

Structure of the read control unit 10 in the input buffer unit 100 according to the present embodiment is shown in FIG. 1. With reference to FIG. 1, the read control unit 10 of the present embodiment includes a state control table 11 to be referred to for the reading of a cell from the queue 110, a delay quality class setting table 12 for setting cell reading priority for each priority class indicative of a discard quality class and a delay quality class assigned to an input cell, a table value modifying unit 13 for modifying a set value of the delay quality class setting table 12 as required, and a cell reading unit 14 for determining the priority order based on the delay quality class setting table 12 and the state control table 11 to read a cell. This arrangement provides, in addition to a function of controlling read according to the priority order based on delay quality classes of the respective queues 110, a function of arbitrarily modifying the order of priority of each queue 110. In FIG. 1, illustration is made only of a characteristic part of the structure of the present embodiment and that of the remaining common part is omitted. The read control unit 10 is implemented by a program-controlled LSI or other processing device. The control program is provided as storage in a storage medium such as a magnetic disk or a semiconductor memory.

The delay quality class setting table 12 is a table which stores the order of priority for reading each delay quality class at the queues 110 logically divided into (the number of output ports of the switch unit 210: N).times.(the number of delay quality classes: y-2). FIG. 2 shows structure of the delay quality class setting table 12. Value of the delay quality class setting table 12 can be arbitrarily changed within the range from `2` to `y-1` and a set value is reflected on an initial delay quality class value.

The table value modifying unit 13, with a time slot for modifying a set value of the delay quality class setting table 12 and a time slot for selecting a queue 110 which will send a cell to the switch unit 210 time-divisionally set within a time for sending one cell from each input buffer unit 100 to the switch unit 210, arbitrarily modifies a set value of the delay quality class setting table 12 without affecting selection of a queue 110 which will send a cell to the switch unit 210 by the cell reading unit 14. Detailed description of the operation by the table value modifying unit 13 will be described later.

The cell reading unit 14, at the time of selection of a queue 110 which will send a cell to the switch unit 210, controls read based on delay quality classes according to the state control table as is done in conventional art, as well as selecting a queue 110 whose cell reading priority set at the delay quality class setting table 12 is high among queues 110 where cells are accumulated and reading and sending cells from the queue 110.

The read control unit 130 has a state control table to be referred to for the reading of cells from the queues 110 and controls such that when the number of cells accumulated in each queue 110 exceeds a threshold value, a delay quality class of the queue 110 is upgraded from `2` to `3` or from `3` to `4` and on the reception of an output buffer threshold value exceeding signal from the congestion monitoring unit 230, the value of a delay quality class of a queue 110 corresponding to the output port in question is reduced to "1".

Cell reading is conducted by sequentially confirming whether cells are accumulated in the queues 110 in the descending order of the classes, starting with a queue 110 whose delay quality class is `4`, the highest, and reading cells of a queue 110 of a class in question when cells are accumulated. When there exist a plurality of queues 110 of the same delay quality class where cells are accumulated, one queue 110 is equally selected under round robin priority control, from which cells are read. When no cell is accumulated in queues 110 whose delay quality class values are `4`, `3`, and `2` and cells are accumulated in a queue 110 whose delay quality class value is `1`, idle cells are transmitted to the switch unit 210 without execution of cell reading from the queue 110.

Description will be next made of operation of the ATM cell buffer circuit according to the present embodiment with respect to the same concrete example as that described in the Related Art. More specifically, it is assumed that the respective queues 110 have three delay quality classes which are referred to as Qos#1, Qos#2 and Qos#3, respectively. Assuming that the number of delay quality classes is three, a value of the delay quality class y managed by the read control unit 130 ranges from `1` to `5` and a value of the initial delay quality class to be assigned to the three delay quality classes will accordingly range from `2` to `4`. If at the start of the services, only two of the three delay quality classes need to be used and when at the time of addition of an unused delay quality class, its priority over the existing two delay quality classes is unknown, conditions of using two classes among the initial delay quality class values from `2` to `4` can not be determined. Therefore, it is assumed that a delay quality class with the value of `2` whose reading priority is low is not to be used and delay quality classes with the values of `3` and `4` are to be used. Setting of a delay quality class to be used is conducted by the cell reading unit 14 of the read control unit 10. More specifically, assuming that at the initial state, the initial delay quality class value of Qos#1 is `2`, the initial delay quality class value of Qos#2 is `3` and the initial delay quality class value of Qos#3 is `4`, queues 110 having the delay quality classes Qos#2 and Qos#3 are to be used and a queue 110 having the delay quality class Qos#1 is yet to be used.

Next, at the time of setting of a delay quality class of the service to be newly started between two delay quality classes whose services are being already provided, the table value modifying unit 13 changes, with respect to the queue 110 of the delay quality class Qos#2 whose initial delay quality class value is `3`, the initial delay quality class value to `2` at the delay quality class setting table 12 and with respect to the queue 110 of the delay quality class Qos#1 whose initial delay quality class value is `2`, changes the initial delay quality class value to `3`. Then, the routing of a desired number of connections with respect to the queue 110 of the delay quality class Qos#1 is set to the queue 110 directed to the switch output port [0], the queue 110 directed to the switch output port [1] and the queue 110 directed to the switch output port [2], the new service is started.

The foregoing operation enables addition of service to be newly started between two delay quality classes whose services are being already provided without stopping services which are being already provided or resetting the routing of the connections for such services.

As described in the foregoing, according to the ATM cell buffer circuit and the priority order allocating method at an ATM switching system of the present invention, the priority of reading of cells accumulated at each queue can be arbitrarily modified. When new service is to be added, this enables arbitrary setting of a delay quality class of the service to be added with respect to delay quality classes of services which are already being provided, thereby allowing desired priority to be given to the reading of cells in a queue related to the service. As a result, it is possible to add service having an arbitrary delay quality class without affecting the services which are being already provided.

The present invention also allows arbitrary addition of service whose delay quality class has any positioning with respect to delay quality classes of the existing services within the range of the number of delay quality services prepared at the device. At the time of provision of delay quality service classes in stages, therefore, this eliminates the need of determining the order of provision and a correlation between classes of delay quality services, thereby enabling various services to be flexibly provided.

Although the invention has been illustrated and described with respect to exemplary embodiment thereof, it should be understood by those skilled in the art that the foregoing and various other changes, omissions and additions may be made therein and thereto, without departing from the spirit and scope of the present invention. Therefore, the present invention should not be understood as limited to the specific embodiment set out above but to include all possible embodiments which can be embodies within a scope encompassed and equivalents thereof with respect to the feature set out in the appended claims.

ATM cell buffer circuit and priority order allocating method at ATM switching system

Claims of correspondent: **US6301253**

What is claimed is:

1. An ATM cell buffer circuit which conducts priority control of the order of transmission of ATM cells at the time of occurrence of ATM cell congestion, comprising:
an output buffer type ATM switch that switches ATM cells and an input buffer unit provided for each line;
said output buffer type ATM switch comprising,
a switching unit that switches one of the cells received from said input buffer unit through an input port to a predetermined output port based on routing information assigned to the one cell,
an output buffer unit provided for said output port of said switching unit and having a plurality of buffer memories therein corresponding to an order of priority based on delay quality classes, and
a congestion monitoring unit provided for each output buffer unit that, when the amount of cells accumulated at the buffer memory in said output buffer unit exceeds a threshold value, notifies said input buffer unit, and
said input buffer unit comprising,
a plurality of queues provided divisionally in terms of logic corresponding to the respective output ports of said switching unit of said output buffer type ATM switch and the respective cell reading priority classes, and disposed at said input port of said output buffer type ATM switch to temporarily store an input cell,
a write control unit that queues said input cell to its corresponding queue based on routing information assigned to the input cell, and
a read control unit that selects a queue whose cell reading priority order is the highest among said queues where said cells are accumulated, based on the amount of cells accumulated at each queue and the notification from said congestion monitoring unit, reads a cell from the selected queue and transmits said cell to said switching unit at each timing of transmitting a cell to said output buffer type ATM switch without any substantial stoppage of service,
wherein said read control unit comprises,
a state control table to be referred to for reading said input cell from said queue,
a delay quality class setting table that sets cell reading priority for each priority class indicative of a discard quality class, a delay quality class and an initial delay quality class assigned to an input cell,
a table value modifying unit that modifies a set value of said delay quality class setting table, and
a cell reading unit that determines the order of priority to read said input cell based on said delay quality class setting table and said state control table.

2. The ATM cell buffer circuit as set forth in claim 1, wherein said delay quality class setting table stores the order of reading priority of each delay quality class at said queues logically divided into (the number of output ports of said switching unit: N).times.(the number of delay quality classes: y-2), a set value of which can be arbitrarily modified in the range from `2` to `y-1`.

3. The ATM cell buffer circuit as set forth in claim 1, wherein said table value modifying unit time-divisionally provides, within a time for transmitting said one cell from said input buffer unit to said switching unit of said output buffer type ATM switch, a time slot that modifies a set value of said delay quality class setting table, and a time slot that selects said queue which will transmit a cell to said switching unit to modify a set value of said delay quality class setting table.

4. The ATM cell buffer circuit as set forth in claim 1, wherein
said delay quality class setting table stores the order of reading priority of each delay quality class at said queues logically divided into (the number of output ports of said switching unit: N).times.(the number of delay quality classes: y-2), a set value of which can be arbitrarily modified in the range from `2` to `y-1`, and
said table value modifying unit time-divisionally provides, within a time for transmitting said one cell from said input buffer unit to said switching unit of said output buffer type ATM switch, a time slot that modifies a set value of said delay quality class setting table, and a time slot that selects said queue which will transmit a cell to said switching unit to modify a set value of said delay quality class setting, table.

5. The ATM cell buffer circuit as set forth in claim 1, wherein
sad read control unit, at the time of reading of said input cell from said one of said plurality of queues, when there exists only one said queue of the same priority class where cells are accumulated, reads a cell from the queue and transmits said cell to said switching unit, when there exists said plurality of said queues of the same priority class where cells are accumulated, equally selects one of said queues by round robin priority control to read a cell and transmit said cell to said switching unit, and when no cell is accumulated in each of said queues, transmits an idle cell to said switching unit.

6. The ATM cell buffer circuit of claim 1, wherein said read control unit substantially eliminates resetting of routing connections.

7. The ATM cell buffer circuit of claim 1, wherein said table value modifying unit allows substantially continuous cell traffic.

8. A priority order allocating method of conducting priority control of the order of transmission of ATM cells at the time of occurrence of ATM cell congestion in an ATM switching system, comprising the steps of:
queuing an input cell to its corresponding queue from a plurality of queues based on routing information assigned to the input cell;
selecting a queue from said queues whose cell reading priority order is the highest among said queues where said cells are accumulated based on the amount of cells accumulated at each of said queues, and reading one of said cells from the selected queue at each timing of cell transmission;
switching said cell read from said selected queue to an output port based on routing information assigned to the cell; and
detecting cell congestion of said cell switched to said output port, and notifying said reading step of the cell congestion as congestion information;
wherein said reading step does not require stoppage of service and includes:
setting a cell reading priority for each priority class indicative of a discard quality class and a delay quality class assigned to an input cell to make a delay quality class setting table,
modifying a set value of said delay quality class setting table, and
determining the order of priority to read one of said cells based on said delay quality class setting table and said congestion information.

9. A priority order allocating method as set forth in claim 8, wherein
at said table value modifying step, a time slot that modifies a set value of said delay quality class setting table and a time slot that selects said queue which will transmit said input cell are time-divisionally provided at each timing of a cell transmission.

10. The method of claim 8, wherein said reading step substantially eliminates resetting of routing connections.

11. The method of claim 8, wherein said modifying step allows substantially continuous cell traffic.

12. A computer readable memory having a control program that conducts priority control of the order of transmission of ATM cells at the time of occurrence of ATM cell congestion in a ATM system, said control program comprising the steps of:
queuing an input cell to a corresponding one of a plurality of queues based on routing information assigned to the input cell;
selecting one of said queues whose cell reading priority order is the highest among said queues, where said cells are accumulated based on the amount of cells accumulated at each said queue, and reading one of said cells from the selected queue at each timing of cell transmission;
switching said cell read from said selected queue to an output port based on said routing information assigned to the input cell; and
detecting cell congestion of said cell switched to said output port, and notifying said reading step of the cell congestion as congestion information;
wherein said reading step does not require stoppage of service and includes:
setting cell reading priority for each priority class indicative of a discard quality class and a delay quality class assigned to said input cell to make a delay quality class setting table, modifying a set value of said delay quality class setting table, and
determining the order of priority to read said input cell based on said delay quality class setting table and said congestion information.

13. The computer readable memory having the control program as set forth in claim 12, wherein at said table value modifying step, a time slot that modifies a set value of said delay quality class setting table and a time slot that selects said queue which will transmit said input cell are time-divisionally provided at each timing of a cell transmission.

14. The memory of claim 12, wherein said reading step substantially eliminates resetting of routing connections.

15. The memory of claim 12, wherein said modifying step allows substantially continuous cell traffic.

16. An ATM cell buffer circuit, comprising an input buffer unit that operates without a substantial stoppage of service, said input buffer unit comprising:
a write control unit that receives an input cell and queues said input cell into one of a plurality of queues in accordance with routing information of said input cell, each of said queues having a reading priority order; and
a read control unit that selects one of said queues having the highest reading priority order among said queues, reads a cell from said selected queue, and transmits said cell to an output buffer type ATM switch that switches said ATM cells, said read control unit comprising,
a state control table configured for reading said read cell from said selected queue,
a delay quality class setting table that sets said a reading priority for each priority class in accordance with a discard quality class and a delay quality class assigned to said input cell,
a table value modifying unit that is coupled to said delay quality class setting table and modifies said reading priority, and
a cell reading unit that is coupled between said state control table and said delay quality class setting table and determines said reading priority order in accordance with said state control table and said delay quality class setting table.

17. The ATM cell buffer circuit of claim 16, wherein said read control unit operates without substantially stopping conduction of cells.

18. The ATM buffer circuit of claim 16, wherein said read control unit substantially eliminates a need to reset routing connections.

19. The ATM buffer circuit of claim 16, wherein said table value modifying unit time-divisionally generates a first time slot that modifies a set value of said delay quality class setting table, and a second time slot that selects said queue to transmit a cell to said output buffer type ATM switch to modify said set value without stopping cell traffic.

20. The ATM buffer circuit of claim 16, wherein:
said read control unit transmits a cell from one of said queues to said output switch when there is only one queue for a priority class;
said read control unit selects a queue by round robin priority control and transmits a cell from said selected queue from one of said queues to said output switch when a plurality of queues exists for said priority class; and
said read control unit transmits an idle cell when said selected queue contains no cell.

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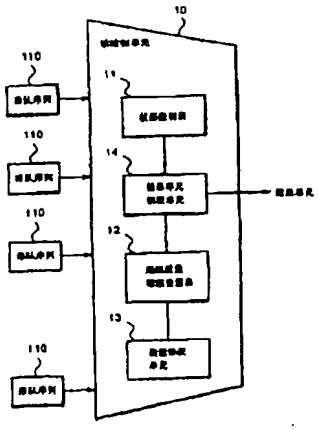
[54]发明名称 ATM缓冲电路及ATM交换系统优先顺序分配方法

[57]摘要

一个 ATM 信息单元缓冲电路包括用于交换 ATM 信息单元的输出缓冲型 ATM 交换单元和提供给每条线的输入缓冲单元，从暂时存储输入信息单元的排队序列中读取信息单元和传送其含有状态控制表的输出缓冲型 ATM 交换机的读取控制装置，对指派给输入信息单元的每个优先级别设置信息单元读优先级的延迟质量等级设置表，修改装置以及基于延迟质量等级设置表和状态控制表确定要读取的信息单元的优先级顺序的读取装置。



权 利 要 求 书

1、一个在ATM信息单元拥挤发生时处理ATM信息单元的传输顺序优先级控制的ATM信息单元缓冲电路，其特征在于包括：

一个用于交换ATM信息单元的输出缓冲型ATM交换机和为每条线提供的一个输入缓冲单元，

所述输出缓冲型ATM交换单元包括：

用来基于指定给信息单元的路线信息交换来自每个输入缓冲单元的信息单元经过输入端口到予先确定的一输出端口的交换装置，

为每个所述交换所装置的每个输出端口提供的并具有基于延迟质量等级对应于优先级顺序的多个缓冲存储器的输出缓冲装置，以及

为每个所述输出缓装置提供的拥挤监视装置，其在所述缓冲装置中缓冲存储器信息单元累计量超过一阀值时，宣告所述超值的输入缓冲单元，以及

所述输入缓冲单元包括：

按照逻辑对应于所述输出缓冲型ATM交换机的所述交换装置的各个输出端口和各个信息单元读取优先等级类别分别提供的并且配置在用于暂存一输入信息单元的所述输出缓冲型ATM交换机的所述输入端口的排队序列，

基于指派给该信息单元的路线信息用于将所述输入信息单元排到其对应的排队序列的写控制装置，以及

读控制装置，其用来基于在每个所述排队序列中信息单元累计的数量和来自所述拥挤监视装置的通知，在信息单元累计的所述排队序列之间选择一个信息单元读取优先级顺序是最高的一排队序列，读取一个来自该选定排队序列的一信息单元以及在传送一信息单元到所述输出缓冲型ATM交换机的时刻将其传送到所述交换装置，

其中所述读控制装置包括：

一个与来自所述排队序列的信息单元的读取有关的状态控制表，

一个为指派给一输入信息单元的表示废弃质量等级和延迟质量等级的优先级别指示而设置信息单元读取优先级的一延迟质量等级设置表，

按需要用于修改所述延迟质量等级设置表的一设定值的表值修改装置，以及

基于所述延迟质量等级设置表和所述状态控制表而用于确定要读取信息单元的优先级顺序的信息单元读取装置。

2、根据权利要求1所述的ATM信息单元缓冲电路，其特征在于：

所述延迟质量等级设置表存储在所述排队序列被逻辑地分为（交换装置的输出端口数：N）×（延迟质量等级数：y－2）时每个延迟质量等级的读优先级顺序，其设定值能够在‘2’到‘y－1’的范围内任意修改。

3、根据权利要求1所述的ATM信息单元缓冲电路，其特征在于：

所述表值修改单元，在用于传送一个信息单元从所述输入缓冲单元到所述输出缓冲型ATM交换装置时间内，时分地提供一个用于修改所述延迟质量等级设置表的设置值的时间间隙和提供一个用于选择所述将要传送一信息单元到所述交换装置的排队序列以修改所述延迟质量等级设置表的一设定值的时间间隙。

4、根据权利要求1所述的ATM信息单元缓冲电路，其特征在于：

所述延迟质量等级设置表存储在所述排队序列被逻辑地分为（交换装置的输出端口数：N）×（延迟质量等级数：y－2）时每个延迟质量等级的读优先级顺序，其设定值能够在‘2’到‘y－1’的范围内任意修改，和

所述表值修改单元，其在用于传送一个信息单元从所述输入缓冲单元到所述输出缓冲型ATM交换机的交换装置的时间内，时分地提供一个用于修改所述延迟质量等级设置表的设定值的时间间隙和提供一个用于选择所述将要传送一信息单元到所述交换装置的排队序列以修改所述延迟质量等级设置表的一设定值的时间间隙。

5、根据权利要求1所述的ATM信息单元缓冲电路，其特征在于：

在自所述排队序列读取信息单元的时间，

当仅存在一个所述同样优先级别的累计信息单元的排队序列时，所述的控制装置从该排队序列中读一个信息单元并传送同样信息单元到所述交换装置，

当存在多个所述同样优先级别的累计信息单元排队序列时，所述的控制装置用圆形优先级控制等同地选择一个所述排队序列去读取一个信息单元并传送它到所述交换装置，以及

当没有信息单元在每个排队序列中累计时，所述的控制装置传送一个空载信息单元到所述交换装置。

6、在一ＡＴＭ交换系统中当发生ＡＴＭ信息单元拥挤时处理ＡＴＭ信息单元传送顺序的优先级控制的一种优先级顺序分配方法，其特征在于包含下列步骤：

基于分派给输入信息单元的路线信息将一个输入信息单元排到它的对应排队序列；

基于每个所述排队序列累计信息单元的量在所述累计信息单元的排队序列之间选定一个信息单元读取优先级最高的排队序列，并且在传送信息单元的每个时间从选定的排列序列读取一个信息单元；

基于指派给该信息单元的路线信息交换所述读自所述选定排队序列的信息单元到一个输出端口；以及

检测交换到所述输出端口的所述信息单元的信息单元拥挤情况并报告所述该信息单元拥挤的所述读取步骤为一拥挤信息；

其中所述读取步骤包括

对表示每个分派给一输入信息单元的废弃质量等级和延迟质量等级的优先级别选择信息单元读取优先级去制作一延迟质量等级设置表，

按需要修改所述延迟质量等级设置表的设定值，以及

基于所述延迟质量等级设置表和所述拥挤信息来确定要读取的信息单元的优先级顺序。

7、根据权利要求6所述的一种优先级顺序分配方法，其特征在于：

在所述表值修改步骤，一个用于修改所述延迟质量等级设置表的设置值的时间间隙和一个用于选定所述将要传送一信息单元的排列序列的

时间间隙被时分地提供在传送信息单元的每一时间。

8、一个计算机可读存储器，其具有用于在ATM系统中ATM信息单元拥挤发生时处理ATM信息单元传送顺序的优先级控制的控制程序，其特征在于所述控制程序包含下面步骤：

基于分派给输入信息单元的路线信息将一个输入信息单元排到它的对应排队序列；

基于在每个所述排队序列累计的信息单元的量在所述累计了信息单元的排队序列之间选定一个信息单元读取优先级最高的排队序列，并且在传送信息单元的每个时间从选定的排列序列读取一个信息单元；

基于指派给该信息单元的路线信息将所述读自所述选定排队序列的信息单元交换到一个输出端口；以及

检测交换到所述输出端口的所述信息单元的信息单元拥挤情况并报告所述信息单元拥挤的所述读取步骤作为一拥挤信息；

其中所述读取步骤包括：

对表示每个分派给一输入信息单元的废弃质量等级和延迟质量等级的优先级别指示选择信息单元读取优先级去制作一延迟质量等级设置表，

按需要修改所述延迟质量等级设置表的设定值，以及

基于所述延迟质量等级设置表和所述拥挤信息确定要读取的信息单元的优先级顺序。

9、根据权利要求8所述的具有控制程序的计算机可读存储器，其特征在于

在所述表值修改步骤，一个用于修改所述延迟质量等级设置表的设置值的时间间隙和一个用于选择所述将要传送--信息单元的排队序列的时间间隙被时分地提供在传送信息单元的每一时刻。

说　　明　　书

ＡＴＭ缓冲电路及ＡＴＭ交换系统优先顺序分配方法

本发明涉及到一个ＡＴＭ信息单元交换装置，尤其是涉及到ＡＴＭ（异步传输模式）交换系统中的一个ＡＴＭ信息单元缓冲电路和一种优先顺序的分配方法，当ＡＴＭ信息单元拥挤发生时，其进行ＡＴＭ信息单元传送顺序的优先级控制。

常规的ＡＴＭ信息单元缓冲电路的一种是，例如，在日本专利公开号平7-297840中公开的一种ＡＴＭ信息单元缓冲电路，名称是“输出缓冲型ＡＴＭ单元交换机中优先级控制方法”。在该文献中叙述的ＡＴＭ信息单元缓冲电路，它其被安装在一个ＡＴＭ交换系统中位于交换单元前级的输入线路单元，它根据每次连接所需的信息单元废弃率和信息单元传送延迟时间限制，使在ＡＴＭ交换系统中处理信息单元废弃率下降并控制各信息单元传输延迟。

图４是一个常规ATM信息单元缓冲电路的结构方框图。如图４所示，ATM缓冲电路包括一个为每条线路提供的输入缓冲单元100和一个输出缓冲型ＡＴＭ交换机200。输入缓冲单元100基于指派给一输入信息单元作为一参数的废弃质量等级和延迟质量等级处理优先级控制。输出缓冲型ATM交换机200基于存在一信息单元的路线信息（输出端口编号和其它信息）处理交换。该交换机还根据输出侧传输容量输出一个信息单元。

输出缓冲型ATM交换机200包括一个交换单元210，输出缓冲单元220和接到各自的输出缓冲单元的拥挤监视单元230。交换单元210基于指派给单元的线路信息交换（自交换）一个经过输入端接收的来自每个输入缓冲器100的信息单元到预定的输出端口。输出缓冲单元220是为交换单元210的每个输出端口提供的，并且它有一组基于延迟质量等级对应于优先级顺序的缓冲存储器。拥挤监视单元230是提供给每个输出缓冲220并且当累计在每个输出缓冲单元220的缓冲存储器中的信息单元数量超过一预定的阀值时，它输出一个输出缓冲器阀值超过信号SO。该输出缓冲阀值超过信号SO从拥挤监视单元230输出反馈到输入缓冲单元100。

输入缓冲单元１００包括一个写控制单元１２０，排队序列１１０和读控制单元１３０。排队序列１１０是在缓冲存储器中，对应于延迟质量等级和交换单元２１０的每个输出端口，为暂时存储一输入信息单元而虚拟提供的逻辑排队。写控制单元１２０根据在每个排队序列１１０中累计信息单元的数量写一个输入信息单元到对应于一延迟质量等级和指派给该输入信息单元的输出端口号的一排队序列。读控制单元１３０接收在每个排队序列１１０累计信息单元量的输入并且接收来自拥挤监视单元２３０的输出缓冲阀值超过信号ＳＯ，并根据输出缓冲阀值超出信号ＳＯ读取并传送来自预定的排队序列１１０的信息单元到交换单元２１０。

图５是一个依据图４中ＡＴＭ单元缓冲电路中延迟质量等级用来描述读优先级顺序的图。参照图５，指派给一输入信息单元的废弃质量等级和延迟质量等级是用一个优先级别矩阵ＣＬ（ｘ，ｙ）来表示。该图显示分配给输入信息单元的废弃质量等级Ｘ越低，要废弃的信息单元越可靠而具有较高废弃率，与其相反，废弃质量等级ｘ越高，要废弃的信息单元可靠性越小而具有低废弃率。该图还显示出延迟质量等级ｙ越低，要读取的信息单元越难并具有较长时间延迟，与之相反，延迟质量等级ｙ越高，要读取的信息单元越容易并具有较短的延迟时间。

下面将参照图５描述输入缓冲单元１００中读控制单元１３０的工作。在每个输入缓冲单元１００，排队序列１１０是逻辑地分为（交换单元２１０的输出端口的编号：Ｎ）Ｘ（初始延迟质量等级的编号：ｙ－２）。假定图５中延迟质量等级是‘１’到‘４’，每个排队序列的初始延迟质量等级是在ＡＴＭ交换机的初始设置时固定地定为“２”或“３”。这个值不能修改。

读控制单元１３０有一个与从排队序列１１０读信息单元有关的状态控制表，并且控制致使当在每个排队序列１１０中信息单元累计的数量超过一个阀值时，排队序列１１０的延迟质量等级从‘２’升到‘３’或从‘３’升到‘４’，并在来自拥挤监视单元２３０的输出缓冲器阀值超出信号的接收上，对应于所讨论的输出端口的排队序列１１０的延迟质量等级值减少到‘１’。接下来执行信息单元读操作确认在排队序列１１０中累计的信息单元是否以降序的形式排列，以一个延迟质量等

级为最高的‘4’的排队序列110起始，并且在信息单元累计时读取讨论的该类排队序列的信息单元。当存在多个信息单元累计的相同延迟质量等级的排队序列110时，一排队序列110在图形优先级控制下从要被读的信息单元中选出。当在排队序列110中没有那些累计延迟质量等级值是‘4’，‘3’和‘2’的单元，并且排列序列110有信息单元累计是延迟质量等级值‘1’，则空载的信息单元传送到交换单元210而没有从排队序列110读取信息单元的操作。

然而，上述常规的ATM信息单元缓冲电路有一个缺点，即在提供服务的一种状态中没有使用ATM信息单元交换装置具有的全部延迟质量等级，当将一个新的延迟质量等级的服务加入时，如果要被分配到附加服务的延迟质量等级与没有采用的延迟质量等级配合失败，象暂停已经提供的延迟质量等级的服务或者重新联接这样的艰苦工作是必需的，这是因为对于从相应排队序列110读取信息单元的优先级相对位置是固定的。

将参照一个具体的例子做进一步的描述。假定在输入缓冲单元100的各个排队序列分别有三个称为Qos#1，Qos#2和Qos#3的延迟质量等级。假定排队序列110的延迟质量等级数是3，由读控制器130管理的延迟质量等级Y的值范围是从‘1’到‘5’，而分配给三个延迟质量等级初始延迟质量等级的值将按照从‘2’到‘4’的范围。如果在服务开始时，三个延迟质量等级中仅有两个需要采用而当未采用的延迟质量等级加入时，其优先级超过存在的两个延迟质量等级是未知的，则不能够确定在初始延迟质量等级值从‘2’到‘4’之间被用两个等级的条件。因此，假设一个具有优先级较低的“2”值的延迟质量等级不被采用而具有‘3’和‘4’值的延迟质量等级被采用。如上述，还可以假定在常规技术中在延迟质量等级Qos#1，Qos#2和Qos#3和初始延迟质量等级值‘2’到‘4’之间的相符在每个排队序列是固定的，且Qos#1的初始延迟质量等级是‘2’，Qos#2的初始延迟质量等级值是‘3’以及Qos#3的初始延迟质量等级值是‘4’。换句话，在服务启始时，具有延迟质量等级Qos#2和Qos#3的排队序列110是被采用，而具有延迟质量等级Qos#1的一排队序列110也还要被使用。

在这些条件下，例如，当相对于已经提供服务的延迟质量等级Qos#2的一个排队序列110，总计300个联接要选路线，对于一个直到交换输出端口（0）的排队序列110是100，对于一个直接到交换输出口（1）的排队序列110是100，以及对于一个直接到交换输出口（2）的排列序列110是100，那么在已提供两个延迟质量等级的服务之间要设置一个新启动的服务延迟质量等级，下面过程是必不可少的。

首先，暂时停止为延迟质量等级Qos#2的排队序列110的所有300个联接服务（信息单元处理）。然后，重新对直接到交换输出端口（0）的延迟质量等级Qos#1的排队序列110，直接到交换输出端口（1）的相同类别的排队序列110和直接到交换输出端（2）的相同类别的排队序列110设置300个联接路线。接下来，恢复这些服务（信息单元处理），并进一步为新的服务设置对直接到相应交换输出端口的延迟质量等级Qos#2的排队序列110的联接路线去启动新的服务。

本发明的一个目的是提供一个ATM信息单元缓冲电路和一种在ATM交换系统上的优先级顺序分配方法，其使新延迟质量等级服务的加入而不停止存在的服务，不考虑该服务新延迟质量等级的定位。

根据本发明的第一方面，一个在ATM信息单元拥挤发生时能处理ATM信息单元传输的顺序的优先级控制的ATM信息单元缓冲电路包括

一个用于交换ATM信息单元的输出缓冲型ATM交换机和一个为各线提供的输入缓冲单元，

该输出缓冲型ATM交换机包括：

基于指派给信息单元的线路信息用于将经过一输入端口自每个输入缓冲单元接收的一个信息单元交换到一预定的输出端的交换装置，

为该交换装置的每个输出端口提供的并且具有基于延迟质量等级对应于优先顺序的多个缓冲存储器的输出缓冲装置，以及

当输出缓冲装置中缓冲存储器累计的信息单元数量超过一定阀值时，通知超值的输入缓冲单元的为每个输出缓冲装置提供的拥挤监视装置，

该输入缓冲单元包括：

按照逻辑对应于输出缓冲型ＡＴＭ交换机的交换装置的各个输出端口和各个信息单元读取优先等级类别分别提供的并且配置在用于暂存一输入信息单元的输出缓冲型ＡＴＭ交换机的输入端口的排队序列，

基于指派给输入信息单元的路线信息用于将输入信息单元排到其对应的排队序列的写控制装置，以及

读控制装置，其用来基于在每个排队序列中信息单元累计的数量和来自拥挤监视装置的通知，在信息单元被累计的排列序列之间选择一个信息单元读取优先级顺序最高的一个排队序列，读取一个来自该选定排队序列的一信息单元以及在传送一信息单元到输出缓冲型ＡＴＭ交换机的时刻将其传送到交换装置。

其中读控制装置包括：

一个与来自所述排队序列的信息单元的读取有关的状态控制表，

一个为指派给一输入信息单元的表示废弃质量等级和延迟质量等级的优先级别设置信息单元读取优先级的一延迟质量等级设置表，

按需要用于修改该延迟质量等级设置表的一设定值的表值修改装置，以及

基于延迟质量等级设置表和状态控制表而用于确定要读取信息单元的优先级顺序的信息单元读取装置。

在最佳的结构中，延迟质量等级设置表存储在排队序列被逻辑地分为（交换装置的输出端口数：Ｎ）×（延迟质量等级数：ｙ－２）时每个延迟质量等级的读优先级顺序，其设定值能够在‘２’到‘ｙ－１’的范围内任意修改的设定值。

在最佳的结构中，表值修改单元，在用于传送一个信息单元从输入缓冲单元到输出缓冲型ＡＴＭ交换装置时间内，时分地提供一个用于修改延迟质量等级设置表的一设置值的时间间隙和提供一个用于选择将要传送一信息单元到交换装置的排队序列以修改延迟质量等级设置表的一设定值的时间间隙。

在另一个最佳结构中，延迟质量等级设置表存储在排队序列被逻辑地分为（交换装置的输出端口数：Ｎ）×（延迟质量等级数：ｙ－２）时每个延迟质量等级的读优先级顺序，其设定值能够在‘２’到‘ｙ－１’的范围内任意修改。以及表值修改单元，其在用于传送一个信息单元

从输入缓冲单元到输出缓冲型ＡＴＭ交换机的交换装置的时间内，时分地提供一个用于修改延迟质量等级设置表的设定值的时间间隙和提供一个用于选择将要传送一信息单元到交换装置的排队序列以修改延迟质量等级设置表的一设定值的时间间隙。

在另一最佳的结构中，在一个来自排队序列的信息单元的读取时间，当仅存在一个同样优先级别的累计了信息单元的排队序列时，读控制装置从该排队序列中读一个信息单元并传送该信息单元到交换装置，当存在多个同样优先级别的累计了信息单元的排队序列时，用圆形优先级控制等同地选择一个排队序列去读取一个信息单元并传送它到交换装置，以及当没有信息单元在每个排队序列中累计时，传送一个空载信息单元到交换装置。

根据本发明的第二方面，在一ＡＴＭ交换系统中当发生ＡＴＭ信息单元拥挤时处理ＡＴＭ信息单元传送顺序的优先级控制的一种优先顺序分配方法，包含下列步骤：

基于分派给输入信息单元的路线信息将一个输入信息单元排到它的对应排队序列，

基于每个排队序列累计信息单元的量在累计信息单元的排队序列之间选定一个信息单元读取优先级最高的排队序列，并且在传送信息单元的每个时间从选定的排队序列读取一个信息单元。

基于指派给该信息单元的路线信息将自选定的排队序列读出的信息单元交换到一个输出端口，以及

检测交换到输出端口的信息单元的信息单元拥挤情况并报告该信息单元拥挤的读取步骤作为一拥挤信息。

其中读取步骤包括：

对表示每个分派给一输入信息单元的废弃质量等级和延迟质量等级的优先级别选择信息单元读取优先级去制作一延迟质量等级设置表。

按需要修改延迟质量等级设置表的设定值，

基于延迟质量等级设置表和拥挤信息来确定要读取的信息单元的优先级顺序，

在这种情况下，在表值修改步骤，一个用于修改延迟质量等级设置表的设定值的时间间隙和一个用于选定将要传送一信息单元的排队序列

的时间间隙被时分地提供在传送信息单元的每一时间。

根据本发明的另一方面，一个计算机可读存储器具有用在ＡＴＭ系统中ＡＴＭ信息单元拥挤发生时处理ＡＴＭ信息单元传送顺序的优先级控制的控制程序，该控制程序包含下列步骤：

基于分派给输入信息单元的路线信息将一个输入信息单元排列到它的对应排队序列；

基于在每个排队序列累计的信息单元的量在累计了信息单元的排队序列间选定一个信息单元读取优先级最高的排队序列，并且在传送信息单元的每个时间从选定的排列序列读取一个信息单元；

基于指派给信息单元的路线信息将自选定排队序列读取的信息单元交换到一个输出端口；及

检测交换到输出端口的信息单元的信息单元拥挤情况并报告信息单元拥挤的读取步骤作为一拥挤信息；

其中读取步骤包括：

对表示每个分派给一输入信息单元的废弃质量等级和延迟质量等级的优先级别选择信息单元读取优先级去制作一延迟质量等级设置表，

按需要修改延迟质量等级设置表的设定值，

基于延迟质量等级设置表和拥挤信息确定要读取的信息单元的优先级顺序。

本发明的其它目的、特征和优点从下面给出的详细描述将会变得更清楚。

从下面给出的详细描述以及本发明所提实施例的附图将会更清楚地了解本发明，然而这并不限制本发明，仅仅是为了说明和理解本发明。

在附图中：

图１是显示根据本发明的一实施例的一个ＡＴＭ信息单元缓冲电路的读取控制单元的结构方框图。

图２是显示本实施例的一个延迟质量等级设置表的结构图。

图３是显示在本实施例中读控制单元内部操作和信息单元传递处理之间关系的一时序图。

图４是ＡＴＭ信息单元缓冲电路的结构方框图。

图５是显示基于延迟质量等级读取优先级顺序的示图。

本发明所提实施例将参照附图在后面给出详细的描述。在下面的描述中，大量特殊细节描述是为了提供对本发明的全面地理解。然而，很明显对于那些在本领域技术上精通的人即使没有这些特殊细节也能够实现本发明。另一种情况，大家熟知的结构没有详细地描述，这是为了不使本发明难以理解。

本发明的一个实施例的ＡＴＭ信息单元缓冲电路类似于图４所示的常规ＡＴＭ信息单元缓冲电路，它包括一个提供给每条线的输入缓冲单元１００和一个输出缓冲型的ＡＴＭ交换机２００。该输出缓冲型ＡＴＭ交换机２００包括一个交换单元２１０，一个输出缓冲单元２２０和一个连接到每个输出缓冲单元的拥挤监视单元２３０，而输入缓冲单元１００包括一个写控制单元１２０，一个排队序列１１０和一个读控制单元１０。除了读控制单元１０外，因为这些元件都与图４所示常规ＡＴＭ信息单元缓冲电路中的对应元件相同，所以同样的参考编号被安排给它们，并略去它们的描述。

根据本发明实施例的输入缓冲单元１００中的读控制单元１０的结构如图１所示。参看图１，本发明实施例的读控制单元１０包括一个涉及到对来自排队序列１１０的一个信息单元读取的一状态控制表１１，一个用于为表示分配给一输入信息单元的废弃质量等级和延迟质量等级的每个优先级设定信息单元读优先级的延迟质量等级设置表１２，一个按需要用于修改延迟质量等级设置表１２的设定值的表值修改单元１３，以及一个用来基于延迟质量等级表１２和状态控制表１１确定优先顺序以读取信息单元的信息单元读取单元１４。除了基于各个排队序列１１０的延迟等级分类而用于根据优先级顺序的一个控制读取功能外，这种结构提供任意地修改每个排队序列１１０的优先级顺序的功能。在图１中，所示出的仅仅是本发明实施例的特殊部分，而其余通用的部分省略了。读控制单元１０是由程序控制的ＬＳＩ或其它处理器件实现的。该控制程序由如磁盘或半导体存储器的存储媒体中的存储器提供。

延迟质量等级设置表１２是一个存储优先级顺序的表格，用于在排队序列被逻辑的分为（交换单元２１０的输出口的数：Ｎ）Ｘ（延迟质量等级数：ｙ－２）时读取每个延迟质量等级。图２显示出延迟质量等级设置表１２的结构。延迟质量等级设置表１２的值能够在范围‘２’

到‘y－1’内任意改变并且设置值反映了是初始延迟质量等级值。

由于用来修改延迟质量等级设置表１２的设定值的时间间隙和用于选择将要传送一信息单元到交换单元２１０的时间间隙时分地设置在从每个输入缓冲单元１００向交换单元２００传送一信息单元的时间内，所以表值修改单元１３任意修改延迟质量等级设置表１２的设定值而不影响经信息单元读单元１４将要传送一信息单元到交换单元２１０的一排队序列１１０的选择。表值修改单元１３运作的详细描述将在后面给出。

在排队序列１１０将要发送一个信息单元到交换单元２１０的选定时间，信息单元读取单元１４如常规技术做的那样依据状态控制表基于延迟质量等级来控制读操作，及选择一个在信息单元被累计的排队序列之中在延迟质量等级设置表１２中信息单元读取优先级设置为高的一排队序列１１０，并从该排队序列１１０中读取和发送信息单元。

读控制单元１３０有一个与从排队序列１１０读取信息单元有关的状态控制表并且控制以使当在每个排队序列１１０中累计的信息单元数超过一阀值时，排队序列１１０的延迟质量等级从“２”升到“３”或从“３”升到“４”，并且根据在来自拥挤监视单元２３０的输出缓冲器阀值超出信号的接收，使对应于所讨论的输出端口排队序列１１０的一延迟质量等级值减少到“１”。在信息单元累计时，信息单元读操作是按顺序地确认在排队序列１１０中信息单元是否是以降序的形式累计的，一个延迟质量等级是“４”的最高的排队序列１１０起始的，和读取所讨论的一类排队序列１１０的信息单元来进行的。当存在信息单元累计的相同延迟质量等级的多个排队序列１１０时，一个排队序列１１０在圆形优先级控制下从读取的信息单元中等同地选出。当延迟质量等级值是“４”，“３”和“２”的排列序列１１０中没有信息单元累计，而其延迟质量等级值是‘１’的排列序列有信息单元累计时，空载的信息单元传送到交换单元２１０而没有从排队序１１０执行读取信息单元的操作。

下面将描述根据已有技术的描述例子相同的本发明实施例的ＡＴＭ信息单元缓冲电路的工作。具体地说，假定各个排队序列１１０有三个延迟质量等级分别是Ｑos#１，Ｑos#２和Ｑos#３。假定延迟质量等级的

数是3个，由读控制单元130安排的延迟等级分类Y的值范围是从“1”到“5”而将被指定分三个延迟质量等级的初始延迟质量等级将相应地安排在‘2’到‘4’的范围。如果在操作开始时，三个延迟质量等级仅仅有两个要被使用，而在不用的延迟质量等级附加的时刻，其超过存在的两个延迟质量等级的优先级是未知的，在初始延迟质量等级从“2”到“4”的值中使用两个级别的情况是不能确定的。因此，假设具有“2”值读优先级的延迟质量等级是低的并不被采用，而具有“3”和‘4’值的延迟质量等级被采用。将被采用的延迟质量等级的设置是由读控制单元10的信息单元读取单元14进行的。具体地说，假定在初始状态，Qos#1的初始延迟质量等级是‘2’，Qos#2的初始延迟质量等级是“3”以及Qos#3的初始延迟质量等级是“4”，具有延迟质量等级Qos#2和Qos#3的序列110将要被采用，而具有延迟质量等级Qos#1的一个排队序列110也还会被采用。

接下来，在已经提供服务的两个延迟质量等级之间将被重新启动的一个延迟质量等级的设置，表值修改单元13，根据初始延迟质量等级值是‘3’的延迟质量等级Qos#2的排队序列，改变在延迟质量等级设置表12的初始延迟质量等级值到‘2’，并根据初始延迟质量等级值是‘2’的延迟质量等级Qos#1的排队序列110，改变这个初始延迟质量等级值到‘3’。然后，对应于延迟质量等级Qos#1的排队序列110的所期望数量的连接的路线被设置到直接对交换输出端口（0）的排列序列110、直接对交换输端口（1）的排队序列110和直接对交换输出端口（2）的排队序列110，新的服务开始。

上述的工作使得在两个已提供服务的延迟质量等级之间重新启动的操作增加并且没有停止已提供的服务或重新对这些服务设置连接的路由。

如上所述，根据本发明的在ATM交换系统上的ATM信息单元缓冲电路和优先级次序分配方法，在各个排队序列上的信息单元累计的读优先级能够任意修改。当新的服务被加入时，这就使得对应于已经提供的服务的延迟质量等级的要被加入的服务的延迟质量等级的设置可以任意，从而使对与该服务有关的排队序列中的信息单元的读取所期望的优先级将给出。结果，可以增加具有任意延迟质量等级的服务而不影响已

经提供的服务。

本发明还允许在该装置上准备的延迟等级服务的数量之内，对应于已存在服务的延迟质量等级的具有任意位置的延迟质量等级的服务的任意增加。因此，在各阶段延迟质量服务等级准备的时刻，这消除了在延迟质量服务等级之间确定准备的顺序和相互关系的需要，所以使得各种服务将被灵活地提供。

虽然本发明已经对于典型的实施例进行了解释的描述，但应该明白对于那些技术精通的人们，是可能做出一些改变、省略和添加，但并没脱离本发明的精神和范围。本发明不应该理解为限制在上述的特殊实施例，应包括所有可能范围内能实施的实施例以及对应于权利要求所陈述特征的等同实施例。

说 明 书 附 图

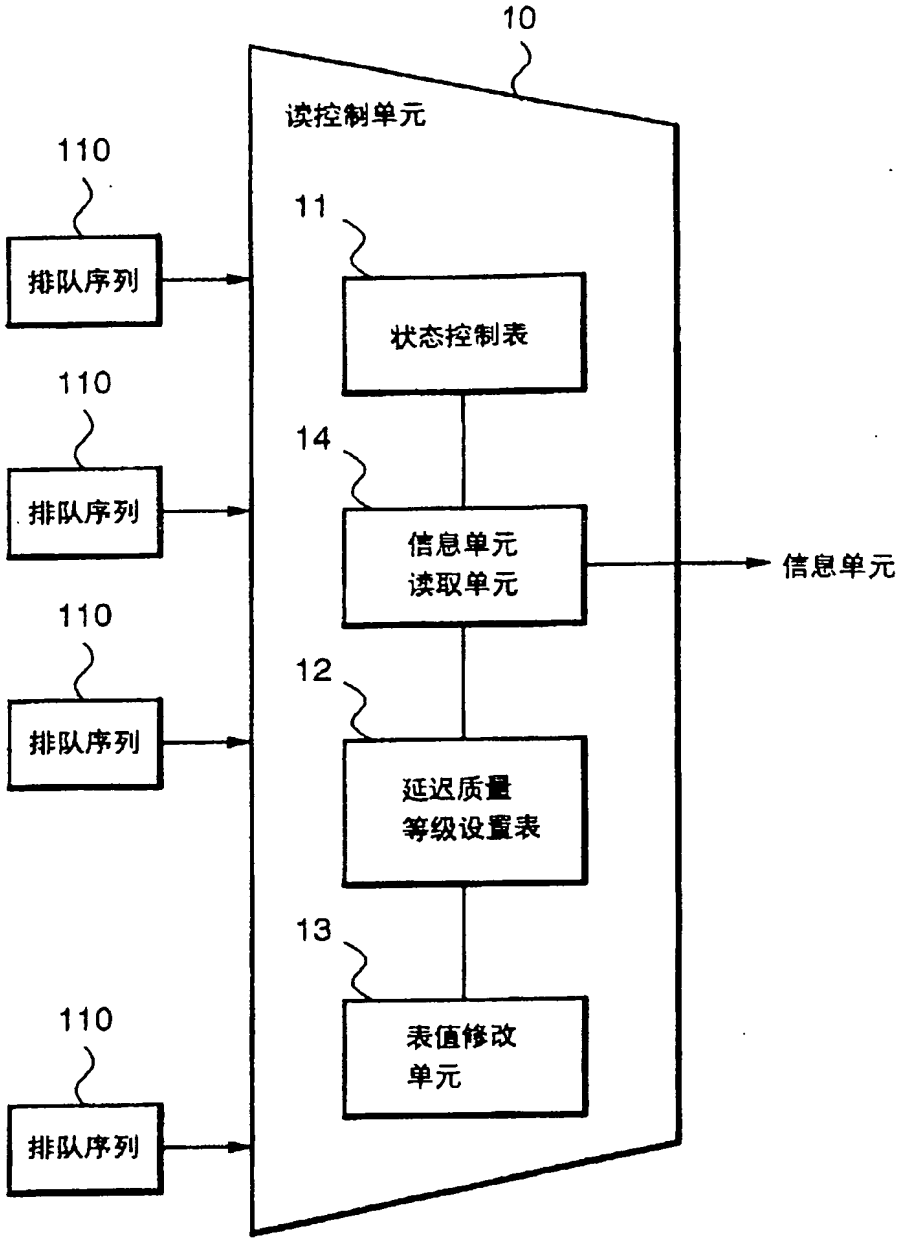

10
读控制单元
110
排队序列
110
排队序列
110
排队序列
110
排队序列
11
状态控制表
14
信息单元
读取单元
12
延迟质量
等级设置表
13
表值修改
单元
信息单元

图 1

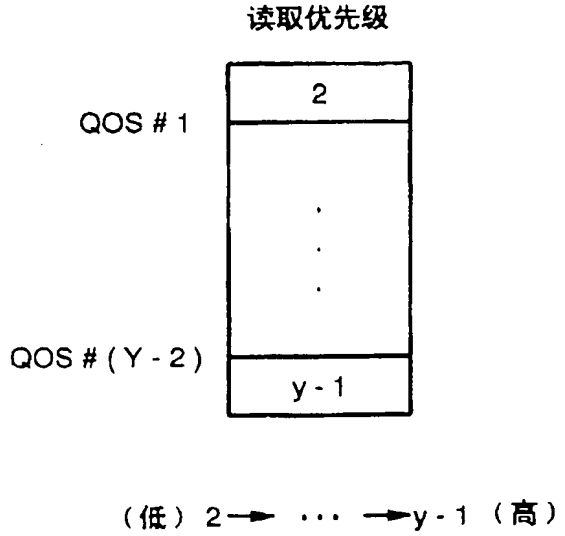
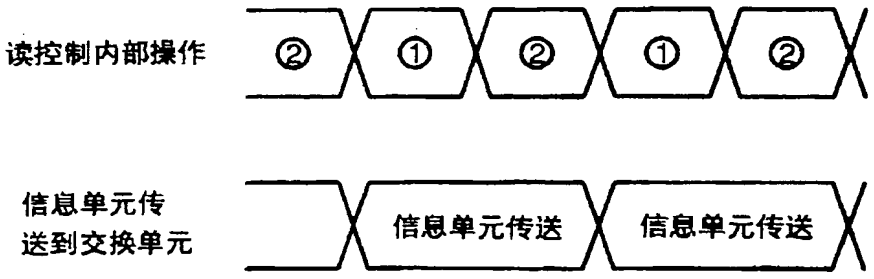


图 2



(1)用于修改延迟质量等级设置表的时间间隙
(2)将要传送信息单元到交换单元的排队序列的选择

图 3

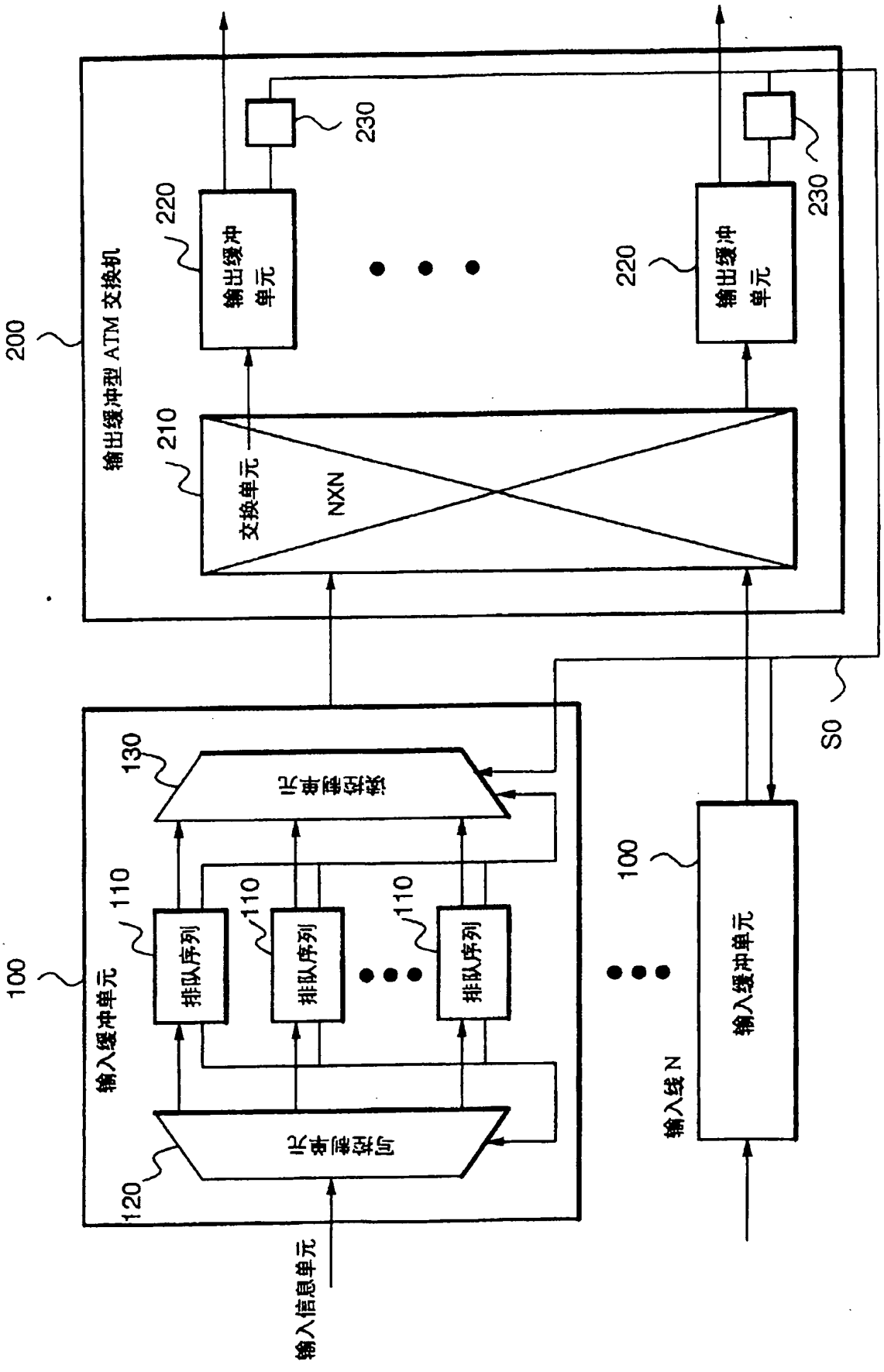

输入信息单元
输入缓冲单元
100
写控制单元
120
排队序列
110
读控制单元
130
输入线 N
输入缓冲单元
100
输出缓冲型 ATM 交换机
200
交换单元
NXN
210
输出缓冲单元
220
230
S0

图 4

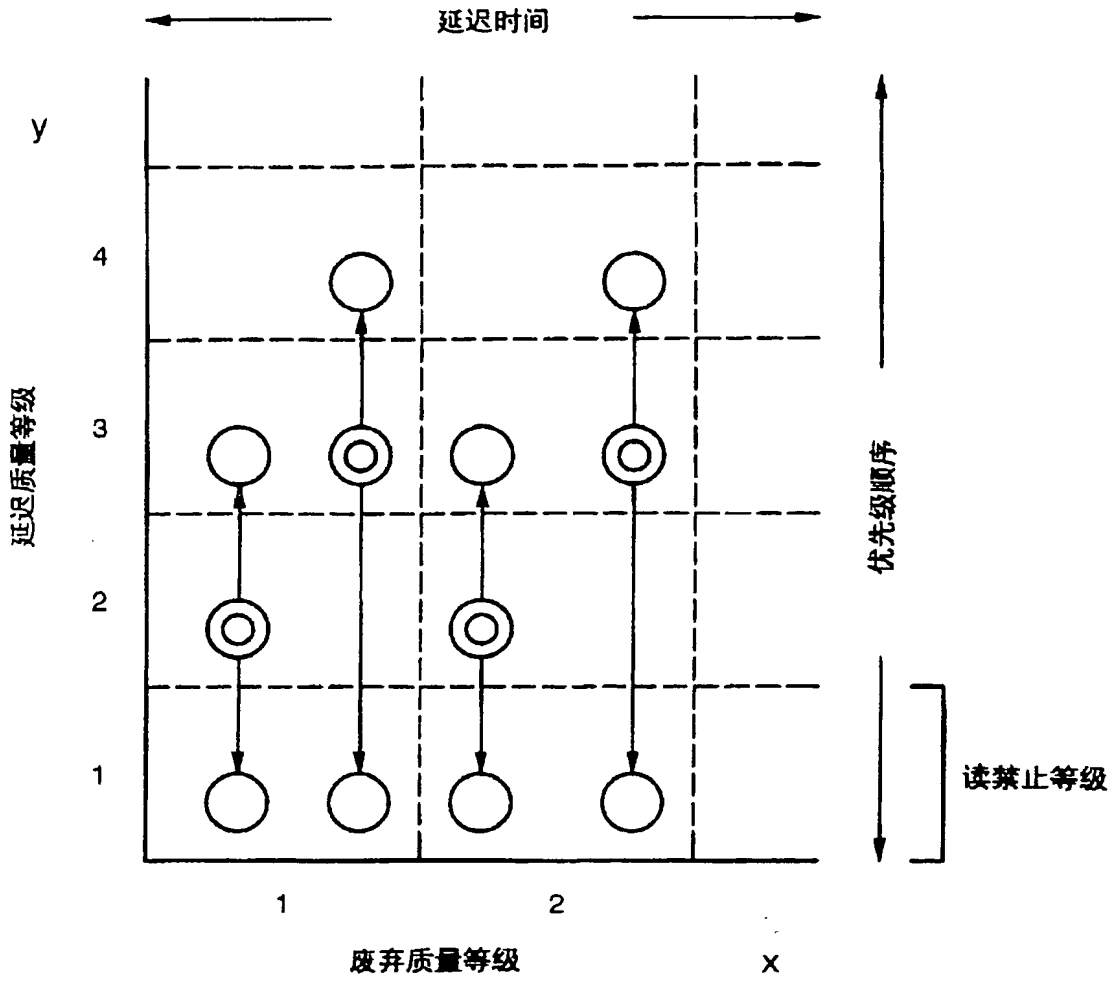


图 5